REMARKS

Applicants respectfully request reconsideration of this application as amended.

Claims 1-38 are pending in the application. Claims 1-32 have been allowed. Claims 33-38 have been rejected.

Claims 1, 2, 17, 18, and 33 have been amended. The amended claims are supported by the specification. No new matter has been added.

A supplemental reissue declaration will be submitted upon the allowance of the claims.

Applicants reserve all rights with respect to the applicability of the doctrine of equivalents.

Claims 33-38 have been rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. The Office Action states that the processor would not be able to know whether the data values in the internal registers have the first or second word size.

Claim 33, as amended, reads as follows.

> A method for context switching a processor that executes procedures having differing word sizes, comprising:
>
> testing a least significant bit of a stack pointer register in the processor that indicates whether a set of data values for a procedure that are stored in a set of registers in the processor each have a first word size or a second word size wherein the first word size is less than the second word size;
>
> transferring the data values from a least significant portion of each register to a first stack save area in memory if the least significant bit of the stack pointer register indicates the first word size;

setting a width indication bit in the first stack save area in memory, and transferring the data values from the registers to a second stack save area in memory if the least significant bit of the stack pointer register indicates the second word size.

Support for claim 33, as amended, can be found throughout the specification including Figures 4A and 4B. Claim 33, as amended, includes the limitation "setting a width indication bit in the first stack save area in memory." Fig. 4A illustrates storing a logic one in LS bit of the 32 bit save area for a stack pointer register if a 64 bit data value is saved. Fig. 4B illustrates reading the same LS bit from the 32 bit save area of the stack pointer register in order to determine if a 32 bit or 64 bit data value has been stored in memory and needs to be restored in the registers of the processor. The processor can access the width indication bit in the first stack save area in order to determine whether the data values in the internal registers have the first or second word size. Accordingly, Applicants respectfully submit that claims 33-38 have not omitted essential steps and request withdrawal of the rejection of claims 33-38 under 35 U.S.C. § 112, second paragraph.

Applicants thank the Examiner for the allowance of claim 1-32.

Claims 1, 2, 17, 18, and 33 have been amended by deleting the phrase "the steps of" from the preamble of each claim in order to better define the invention.

In view of the foregoing amendments and remarks, applicants respectfully submit that all of the rejections and objections have been overcome.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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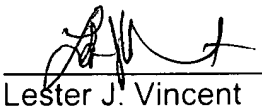

Lester J. Vincent
Reg. No. 31,460

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300